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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,429	10/27/2000	Takenobu Tani	43889-992	4792

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EXAMINER

BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
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2186

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DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/697,429

Applicant(s)

TANI, TAKENOBU

Examiner

Pierre-Michel Bataille

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Correspondence

1. This Office Action is taken in response to Applicant's filed application on October 27, 2000, in which claims 1-9 are pending.
2. The Office acknowledges the filing of Information Disclosure Statements (IDS) filed on the same date as the application and acknowledges claims for priority filed also the same date as the application, whose priority paper has been placed in the application.
3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

The abstract, specification and claims are objected to because the first occurrence of all acronyms or abbreviations in each should be written out for clarity. ROM should be replaced with 'read-only-memory (ROM)' and RAM should be replaced with 'random access memory (RAM)'.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,078,548 (Jih).

With respect to claims 1 and 8, Jih teaches a microprocessor provided with a program modification function [(CPU capable of modifying built-in program codes thereof and method) title; abstract; Fig. 2], comprising: an instruction storage unit including a ROM for storing instructions composing a program to be processed (a read-only memory (ROM) 10 (FIG. 2) for storing program codes) and a modified instruction storage unit for storing a modified instruction for program modification (a random-access memory (RAM) 20 (FIG. 2) for storing a special instruction and modified program codes) [abstract; Fig. 2; Col. 1, Lines 56-61]; an address translation unit (special instruction detecting circuit) for receiving an instruction address of an instruction stored in said ROM and for translating the instruction address into a substitute address at which the modified instruction is stored in said modified instruction storage unit when the instruction address matches with a modified address which is an address of an instruction to be modified [30, FIG. 2; abstract; Col. 2, Lines 5-12], said address translation unit outputting the substitutive address to said instruction storage unit instead of the instruction address (special instruction detecting circuit connected to

the ROM and the RAM to drive the CPU to transfer to read said modified program codes in the RAM when said special instruction is detected) [abstract; Col. 2, Lines 17-21; Col. 4, Lines 20-41].

With respect to claims 3 and 5, Jih teaches said address translation unit composed of a memory which outputs translated addresses in accordance with received instruction address [abstract; Col. 2, Lines 5-12] and address translation unit composed that a bit width to be a translation target is changeable when the instruction address is translated into the substitutive address [abstract; Col. 2, Lines 22-29; Col. 4, Lines 21-47].

With respect to claims 2 and 4, said address translation unit comprising a modifying address storage unit for holding a value of a predetermined bit of the modifying address [Col. 3, Line 6-8, Lines 56-62]; an address comparator for comparing a value of said predetermined bit of the received instruction address with the value held in said modifying address storage unit to determine whether or not these values match (special instruction detecting circuit comprising comparators for comparing said selecting code and a higher bit of the address of the ROM to where the program counter directs) [Fig. 5; Col. Lines 19-34; Col. 4, Lines 20-27]; a substitutive address storage unit for holding a value of said predetermined bit of the substitutive address [Col. 3, Line 56 to Col. 4, Line 9]; and an address selector for receiving determination results of said address comparator, outputting as a value of said predetermined bit of a new instruction address, the value held in said substitutive address storage unit when the received results indicate a match, and otherwise the value of said predetermined bit of the instruction address (a multiplexer for passing the program codes in the ROM to execute in the normal operation, and to be

switched to pass the modified program codes in the RAM to execute when the special instruction is detected) [Col. 4, Lines 1-19]; a translation range setting means capable of setting whether or not said predetermined bit is designated as a translation target bit, said address translation range setting means making said address selector output the value of said predetermined bit of the instruction address, regardless of the determination results of said address comparator (determining number or regions and each region size) [Fig. 8; Col. 5, Lines 1-9].

With respect to claim 6, Jih teaches the address translation unit is composed of a field programmable logic which outputs translated address in accordance with received instruction address [Col 3, Line 62 to Col. 4, Line 9].

With respect to claims 7 and 9, Jih teaches said modified instruction storage unit stores an additional instruction for program modification and further stores a branch instruction having as a branch target an address of the additional instruction (special instruction is written in an address of the RAM corresponding to the memory address, where the program codes are to be replaced, of the ROM) [abstract; Col. 1, Line 59 to Col. 2, Line 12].

Conclusion


6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,274,815 (Trissel et al) teaching dynamic instruction modifying controller and operation method.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.


Pierre-Michel Bataille
Examiner
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